A New Direct Millimeter-Wave Six-Port Receiver

Serioja Ovidiu Tatu, Emilia Moldovan, Ke Wu, *Fellow, IEEE*, and Renato G. Bosisio, *Fellow, IEEE*

***Abstract*—A new direct-conversion wide-band (23–31 GHz) six-port receiver is proposed suitable for millimeter-wave integrated system design. This new hardware receiver is found to be robust, rugged, low cost, and suitable for use in broad-band wireless mass-market QPSK communications. The prototype circuits are fabricated to validate this new concept with our miniaturized hybrid microwave integrated-circuit technology and the proposed receiver topology is also suitable for monolithic-microwave integrated-circuit fabrication. This application-specific integrated receiver is designed on the basis of a wide-band six-port junction and other analogical circuits in the form of a simple multichip module. Bit-error-rate measurements and simulation results are shown and discussed in the presence of noise, adjacent signal interference, local-oscillator (LO) phase shift, and LO phase noise. The maximum bit rate is fundamentally limited by the speed of the video and decoder circuits. Nevertheless, several hundred megabits per second can be achieved at low cost.**

***Index Terms*—Homodyne receiver, MHMIC technology, millimeter wave, QPSK modulation, six-port junction.**

I. Introduction

It is widely recognized that direct conversion receivers offer unique advantages in wireless communications by reducing circuit complexity and allowing a higher level of circuit integration than conventional heterodyne receivers [1]. Six-port direct conversion receivers have been proposed [2]–[5] as multimode or software receivers operating with digital signal processors (DSPs) programmed for a number of modulation schemes.

The idea of using a six-port structure to determinate the phase of a microwave signal was first presented in 1964 by Cohn and Weinhouse [6]. A six-port can be considered as a black box with two inputs and four outputs. The output ports are terminated with power detectors. Characteristic relation or correlation between two input signals (phase and amplitude) can be determined when the relation between the input and output ports becomes known. The only requirements are that the six-port circuitry is linear and that the outputs are nonlinearly dependent on each other. The four unknowns can be obtained from a set of characteristic equations. Those equations can be found very accurately with a calibration procedure. Therefore, the six-port structure has been used in the design of network analyzers and other similar applications. A detailed analysis of the six-port structure can be found in [7].

This paper presents recent results obtained on a new six-port-based hardware-type receiver that is designed with application-specific integrated circuits (ASICs) for QPSK-related communication systems. The proposed millimeter-wave ASIC approach is useful in the design of other similar hardware receivers at higher or lower operating frequencies (microwaves and sub-millimeter waves) using either discrete element [3], [5] or distributed parameter [2], [4] six-ports. This six-port receiver is designed to operate without the need for precise power readings and also without a DSP, as required in the design of previous six-port receivers. The new receiver contains one multichip module (MCM) consisting of a wide-band six-port junction, four RF detectors (based on Schottky diodes), video amplifiers, and one $I\&Q$ decoder. The proposed receiver architecture is to satisfy the requirements of hardware receivers used in high-speed QPSK communications. RF and demodulation test results in the presence of noise, adjacent channel interference, local-oscillator (LO) phase shift, and phase noise are presented at data rates of 40 Mb/s. In this implementation, the maximum bit rate is 58 Mb/s for a bit error rate (BER) less than $1.0E-6$.

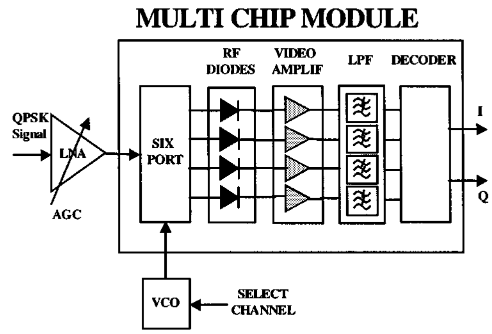

Fig. 1. Complete diagram of the proposed receiver architecture.

II. Receiver Architecture and Operating Principle

Fig. 1 describes the design diagrams of our hardware receiver architecture with a number of circuits incorporated in an MCM to provide I&Q data output channels directly from the received QPSK signals. The principal part of this ASIC is a wide-band six-port junction with two input signals (input unknown QPSK signal and known voltage-controlled oscillator (VCO) signal) and four output signals. After a scalar detection using four zero-bias Schottky diodes, the output signals are amplified and then filtered using video amplifiers and low-pass filters. An analog decoder using a set of comparators provides the I&Q output signals. The input QPSK signal may be going through a low-noise amplifier (LNA) with automatic gain control (AGC), depending on the application requirement and dynamic range of the signal.

The complete RF microstrip topology is shown in Fig. 2 and consists of a wide-band millimeter-wave (Ka-band in our design) distributed parametric six-port junction with surface-mounted RF diodes and related matching circuit networks. The circuit is fabricated in miniaturized hybrid microwave integrated circuit (MHMIC) technology on a 250-μm ceramic

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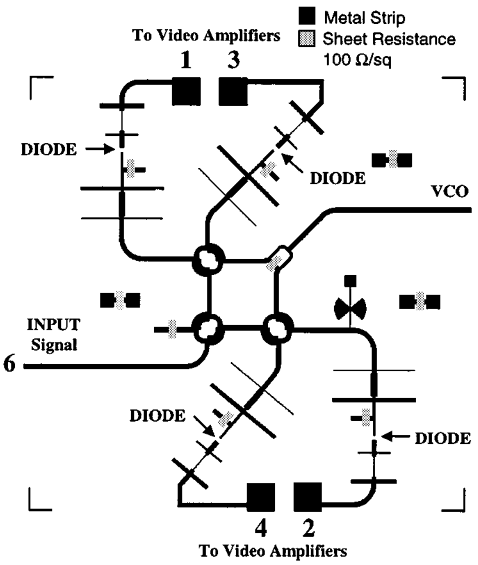

Fig. 2. Design layout of the six-port junction and matching networks for the detector RF circuit.

TABLE I
MEASURED AND SIMULATED S-PARAMETERS OF OUR DESIGNED SIX-PORT JUNCTION AT 27 GHz

S Parameters	Simulations [dB]	Measurements [dB]
S11	- 38.9	- 27.0
S22	- 31.2	- 25.0
S33	- 28.8	- 24.0
S44	- 30.9	- 25.0
S55	- 38.0	- 27.0
S66	- 30.4	- 25.0
S56	- 33.5	- 27.0
S51	- 6.3	- 6.4
S52	- 6.4	- 6.5
S53	- 6.4	- 6.5
S54	- 6.2	- 6.4
S61	- 6.2	- 6.5
S62	- 6.3	- 6.5
S63	- 6.1	- 6.4
S64	- 6.5	- 6.6

substrate with a relative permittivity $\varepsilon_r = 9.9$. The MHMIC chip measures 23 × 23 mm. The six-port junction composed of three compact hybrid 90° couplers and a Wilkinson power divider is placed in the middle of the circuit layout.

Simulated and measured S-parameters of the six-port junction are summarized in Table I, for the center frequency at 27 GHz. The reflection coefficients S_{11}–S_{66} are less than -24 dB and the isolation between LNA and VCO ports, i.e., S_{56}, is found to be at least -27 dB. The transmission coefficients are close to the theoretical predicted value (-6 dB). The circuit of detection is designed to cope with a wide-band operation (23–31 GHz) using HSCH-9161–type zero-bias-detection Schottky diodes.

It is to be noted that a similar architecture can be used for higher operating frequencies in the millimeter-wave frequency band. The six-port junction and matching networks for the detection circuit can be readily designed for the new frequency and bandwidth.

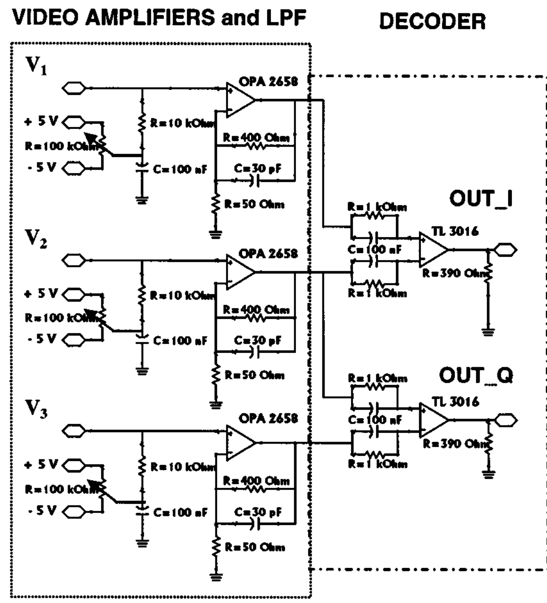

Fig. 3. Block presentation of active integrated LPFs, video amplifiers, and analog decoder circuit used in the receiver.

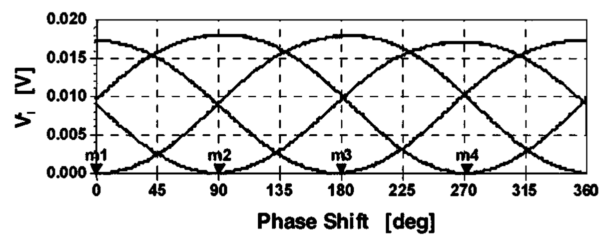

Fig. 4. Output voltage waveforms of the detectors versus the input signal/VCO phase shift.

Fig. 3 shows electronic circuits used for the video amplifiers, integrated active low-pass filters (LPFs) and analog decoder circuits. The active low-pass filters, which make use of an OPA 2658 current feedback operational amplifier, have a cutoff frequency of 100 MHz corresponding to the maximum baseband requirement for the QPSK test signals used. The analog decoder uses two ultrafast low-power precision comparators (TL3016) to provide a high data rate.

The RF design of the six-port junction is such that only one of four possible modulation states is correctly identified at a time by an analog decoder. This is one particular feature of the proposed receiver concept. Waveforms displayed in Fig. 4 indicate that each output voltage of the six-port junction, as shown in Fig. 2, has a single minimum value ($m1$, $m2$, $m3$, $m4$ corresponding to V_1, V_2, V_3, V_4, respectively) during a 360° phase shift between RF input and VCO signals. This means that V_1, V_2, V_3, V_4 have a minimum value for 0°, 90°, 180°, and 270° phase shift, respectively, between the input and VCO signals.

The simulated input and output $I\&Q$ waveforms, as plotted in Fig. 5, confirm the operating principle of the receiver. The input $I\&Q$ signals, IN_I and IN_Q, are pseudorandom bit sequenced at the input of the vector modulator (see Fig. 8). The input phase

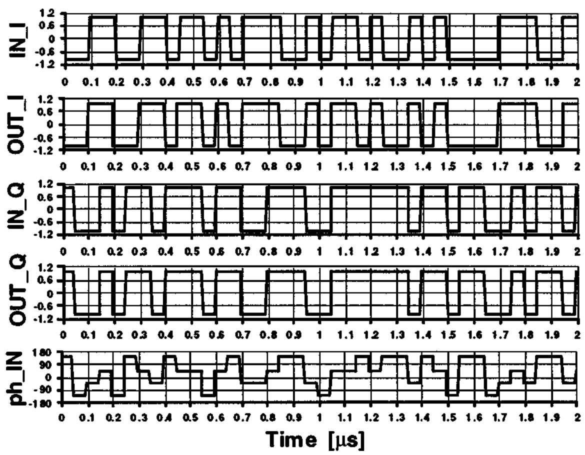

Fig. 5. Simulated input and output $I\&Q$ waveforms of the receiver as a function of time.

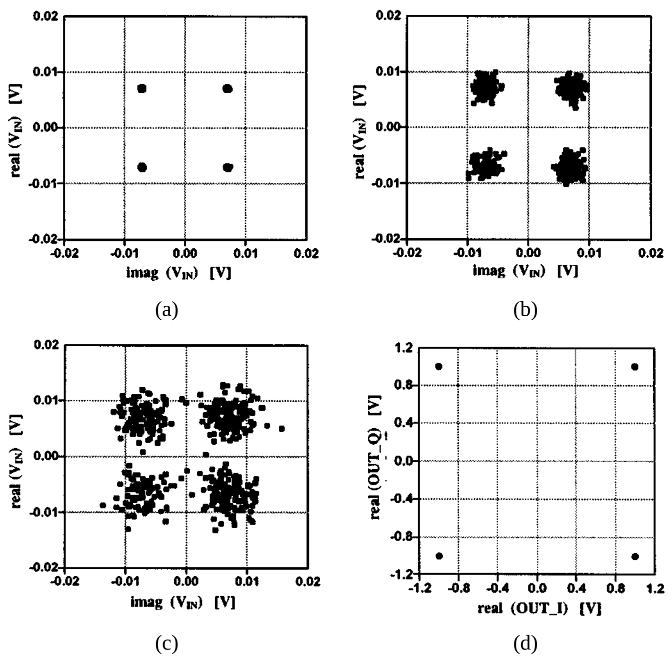

Fig. 6. Simulated input and output signal constellations for different SNRs.

signal $\mathrm{ph}_{\mathrm{IN}}$ is the phase of the QPSK modulated signal. The same bit sequence OUT_I and OUT_Q are obtained at the output of the MCM.

Fig. 6 shows the simulated input and output signal constellations for various signal-to-noise ratios (SNRs). A white noise is added to the input QPSK signal and the input constellations are presented in Fig. 6(a)–(c) for 30-, 10-, and 4-dB SNRs, respectively. Demodulation results are presented in Fig. 6(d), as well, which are obtained by using the comparators in the decoder circuit of Fig. 3. It is found that the output constellation is definitely stable. This output constellation remains focused even if the errors appear because of the comparators in the decoder circuit whose output voltages can have only two distinct values. Otherwise, if the errors appear, the output signal constellation presents a rotation to the left or right of 90° multiplies and "the image" of the output constellation is the same. Therefore, the errors appear in the demodulated signal and the BER rises up.

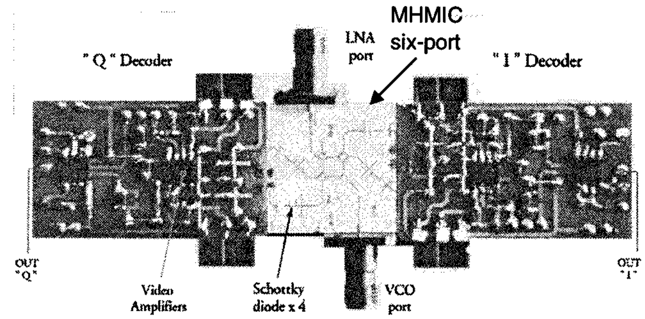

Fig. 7. Complete experimental receiver prototype (measured by 100 mm × 25 mm).

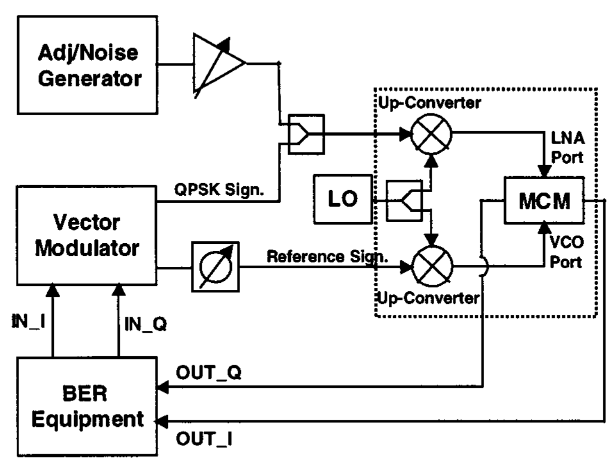

Fig. 8. Measurement setup of the MCM for BER testing.

III. Prototype and Test Results

To validate our proposed receiver and the above analyses, an experimental compact prototype was made. Fig. 7 shows a photograph of the complete circuit module, including an ASIC, as depicted in Figs. 2 and 3, with the six-port junction fabricated using our MHMIC process. Obviously, the front-end of this receiver can be designed in a single chip with a monolithic-microwave integrated-circuit (MMIC) technique to integrate all of the RF components (VCO, LNA, six-port junction, and RF diodes with matching circuits).

The block diagram of the experimental and simulation setup is given in Fig. 8 to measure the BER performance, with respect to signal parameters of the receiver. A pseudorandom bit sequence ($2^{23} - 1$ b) is generated using ME 522A BER transmitter equipment. The bit rate is set at 40 Mb/s. A QPSK modulated signal and a reference signal of 250 MHz are generated using an HP-8782 vector signal generator. The 27-GHz QPSK modulated signal and the 27-GHz reference signal are obtained using an LO (Wiltron frequency synthesizer model 6740B at 26.75 GHz) and two SU26A21D sideband up-converters. The demodulated $I\&Q$ signals are obtained using the MCM, as shown in Fig. 7. The ME 522A BER receiver equipment evaluates the BER values. An additional continuous-wave (CW) generator or a white noise generator is used for the adjacent signal interference or noise measurements.

Fig. 9 shows a photograph of our test setup, as sketched in Fig. 8, which consists of the MCM, a power divider, and two up converters. The BER results using simulations based on the

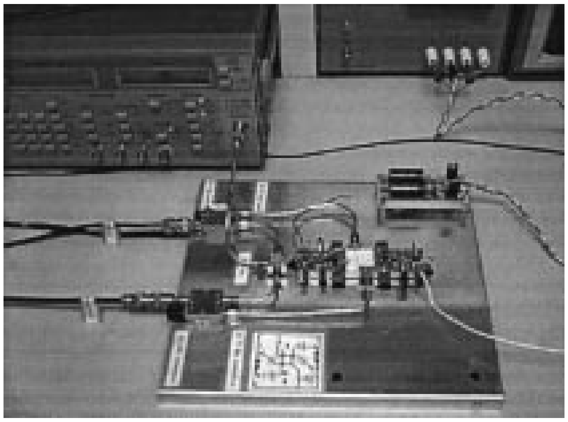

Fig. 9. Our test bed for the evaluation of the receiver performance.

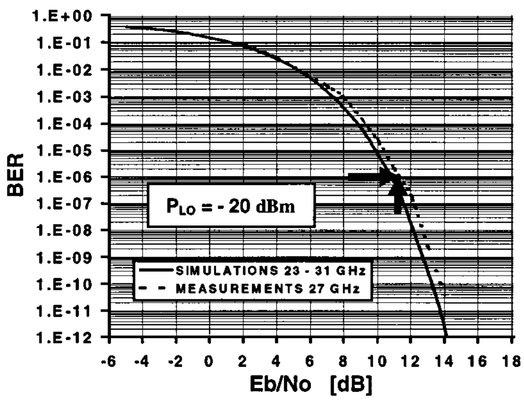

Fig. 10. Measured and simulated BER versus E_b/N_o over the operating band (23–31 GHz).

ADS 1.3 version and measurements are obtained considering the same conditions of power inputs and interferences (white noise, adjacent signal interference, LO phase shift, and LO phase noise).

Fig. 10 shows a simulated and measured BER as a function of E_b/N_O, in which E_b is the average energy of a modulated bit and N_O is the noise power spectral density. The signal is correctly demodulated if the E_b/N_O ratio has an acceptable value. It can be seen that the BER is less than $1.0E-6$ for E_b/N_O once higher than 11 dB over the frequency range within the operating band (23–31 GHz). Outside the upper and lower limits of the operating bandwidth, however, the BER rises rapidly, as it is measured to be greater than $1.0E-4$ at 22 GHz and 32 GHz for the same value of E_b/N_O.

Fig. 11 gives the results of a measured and simulated BER versus the RF signal power level at the LNA port of the MCM, as indicated in Fig. 7, with an LO signal power of -20 dBm. From these results, it can be observed that a minimum signal level of -36 dBm (-16 dBm below the LO signal power) is sufficient to operate the MCM (corresponding to a BER of $1.0E-6$). The maximum power level of the RF input signal is measured to be 3 dBm (+23 dBm above the LO signal power) before the BER rapidly deteriorates up to $1.0E-6$. Hence, the dynamic range of the MCM alone is approximately 40 dB when the LO power level is set at -20 dBm. Therefore, this MCM is a very robust QPSK demodulator according to the dynamic range of the input QPSK signal. The sensibility of the receiver can be

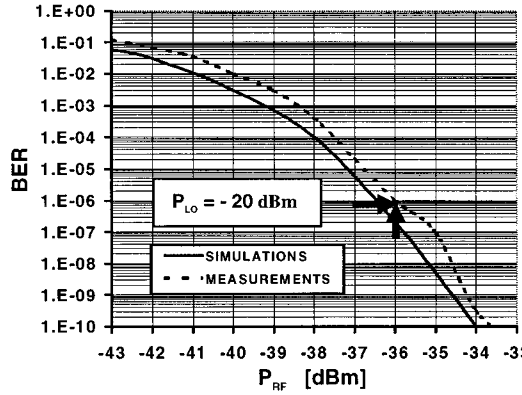

Fig. 11. Measured and simulated BER versus RF power level at the LNA port of Fig. 7 for a carrier frequency of 27 GHz.

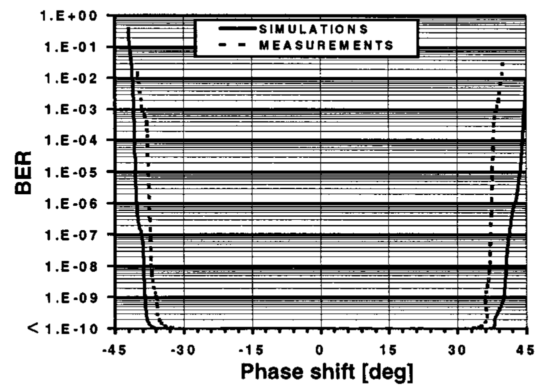

Fig. 12. Measured and simulated BER versus LO phase shift from the synchronism (0°).

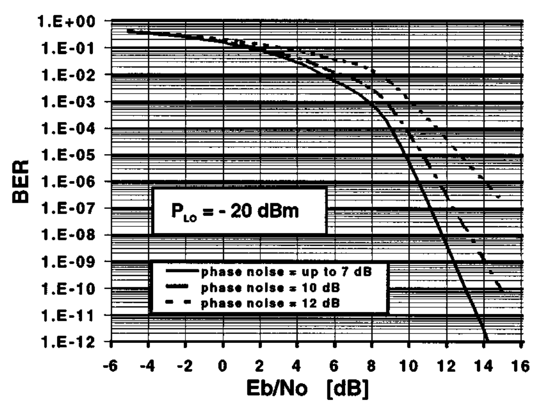

Fig. 13. Simulated BER results versus E_b/N_0 for different LO phase noise levels.

increased using an LNA. The dynamic range of the receiver can also be increased well above 70 dB with an AGC in the LNA.

In addition, Fig. 12 shows simulated and measured results on BER versus the phase shift from synchronism between the carrier and LO signals when both frequencies are set at 27 GHz. The simulated and measured BER is less than $1.0E-6$ for the LO phases shift from the synchronism smaller than $\pm 35^\circ$ and the BER is less than $1.0E-10$ for the LO phases shift from the synchronism smaller than $\pm 30^\circ$. Therefore, this MCM is a very robust QPSK demodulator according to an undesired phase-shift error.

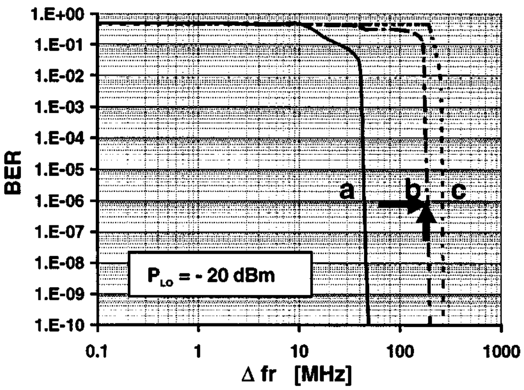

Fig. 14. Measured BER performance versus frequency difference (Δfr) between the carrier (27 GHz) and CW interference signals. Data rate is set at 40 Mb/s and the interference signal power levels above carrier (−20 dBm) are a: 0 dB, b: 3 dB, and c: 6 dB.

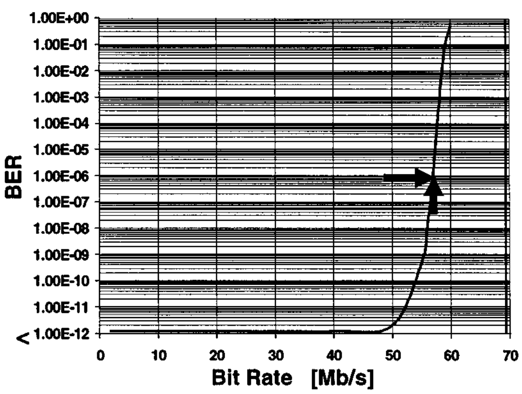

Fig. 15. Measured BER performance versus bit rate used in the receiver evaluation.

Fig. 13 presents a simulated BER versus E_b/N_O for different LO phase noise levels. It is found that the BER curve is identical to the theoretical one for an LO phase noise less than 7 dB.

Fig. 14 gives measured BER results, with respect to amplitude and frequency variations of a CW interference signal using QPSK signals received at a rate of 40 Mb/s. It indicates that the BER is less than $1.0E-6$ when the frequency difference (Δfr) for the interference signal is more than twice the cutoff frequency of an LPF (200 MHz) and its power level is 3 dB above the carrier level (−20 dBm). If the power level of the CW signal increases, for the same amount of frequency difference (Δfr) between the carrier and CW signal, the BER will also increase.

Fig. 15 shows that the maximum acceptable bit rate for our design receiver is 58 Mb/s corresponding to a BER less than $1.0E-6$. This rate is solely limited by the speed of the video and decoder circuits.

IV. Conclusions

A new direct conversion hardware receiver based on six-port technology has been proposed and has been found suitable for low-cost mass-market wide-band millimeter-wave applications. This new receiver presents a viable alternative for mobile terminals. It is shown that the new circuit can effectively operate with low voltage and a low LO power (in this case, −20 dBm). BER results are comparable to a standard direct conversion receiver as the proposed concept is verified by measurements and simulations based on a hybrid integrated-circuit prototype having an operating band of 8 GHz (23–31 GHz).

An analog carrier recovery circuit has been designed, in which a voltage control to a VCO is generated using six-port output signals. It has been found that the four output dc voltage levels change in time if the VCO frequency is different from the carrier RF frequency. This frequency difference is then converted into a dc voltage magnitude using a frequency/voltage converter. The sign of frequency difference is added to this dc voltage and the resulting control voltage signal is fed back to the VCO [8].

The BER results have been studied in the operating dynamic range, signal-to-noise ratio, signal interference, and VCO phase noise. Our simulated and measured results are very encouraging, which pushes forward our current design and future fabrication of a MMIC prototype for this new receiver.

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Dr. Wu is a member of the Electromagnetics Academy. He was chairperson of the 1996 Symposium on Antenna Technology and Applied Electromagnetics (ANTEM) Publicity Committee and vice-chairperson of the Technical Program Committee (TPC) for the 1997 Asia–Pacific Microwave Conference (APMC'97). He has served on the FCAR Grant Selection Committee and the TPC committee for the International Conference on Telecommunications in Modern Satellite Cable and Broadcasting Services (TELSIKS) and International Microwave and Optical Technology (ISMOT). He has also served on the ISRAMT International Advisory Committee. He was the general co-chair of the 1999 and 2000 SPIE International Symposium on Terahertz and Gigahertz Electronics and Photonics, Denver, CO, and San Diego, CA, respectively. He was the general chair of 8th International Microwave and Optical Technology (ISMOT'2001), Montreál, QC, Canada, June 19–23, 2001. He has served on the Editorial or Review Boards of various technical journals, including the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, the IEEE TRANSACTIONS ON ANTENNAS AND PROPAGATION, and the IEEE MICROWAVE AND GUIDED WAVE LETTERS He served on the 1996 IEEE Admission and Advancement (A&A) Committee, the Steering Committee for the 1997 joint IEEE Antennas and Propagation Society (IEEE AP-S)/URSI International Symposium. He has also served as a TPC member for the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) International Microwave Symposium. He was elected to the Board of Directors of the Canadian Institute for Telecommunication Research (CITR). He also serves on the Technical Advisory Board of Lumenon Lightwave Technology Inc. He is currently the chair of the joint IEEE chapters of the IEEE MTT-S/IEEE AP-S/IEEE Lasers and Electro-Optics Society (IEEE LEOS), Montreál, QC, Canada. He was the recipient of the URSI Young Scientist Award, the Institute of Electrical Engineers (IEE), U.K., Oliver Lodge Premium Award, the Asia–Pacific Microwave Prize Award, the University Research Award "Prix Poly 1873 pour l'Excellence en Recherche" presented by the École Polytechnique on the occasion of its 125th anniversary, and the Urgel–Archambault Prize (the highest honor) in the field of physical sciences, mathematics and engineering presented by the French–Canadian Association for the Advancement of Science (ACFAS).

Renato G. Bosisio (M'79–SM'89–F'95) was born on June 28, 1930 in Monza, Italy. He received the B.Sc. degree in mathematics and physics from McGill University, Montreál, QC, Canada, in 1951, and the M.A Sc. degree in electrical engineering from the University of Florida, Gainesville, in 1963.

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Prof. Bosisio is a member of the Sigma Xi Research Society at McGill University, Phi Kappa Phi Learned Society at the University of Florida, and l'Ordre des Ingénieurs du Québec. He was the recipient of a number of awards, including the 1996 IEEE Canada Outstanding Educator Award, the 1973 École Polytechnique Outstanding Professor Award, and the 1971 Canada Patents and Development Limited "The Inventor" Award.